AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims

1. (Original) A semiconductor device, comprising:

a plurality of word lines;

first and second bit lines; and

a plurality of memory cells, each of the plurality of memory cells having first and second P-channel type MISFETs, and third, fourth, fifth, and sixth N-channel type MISFETs,

wherein drains of the first and third MISFETs are connected to gates of the second and fourth MISFETs, gates of the first and third MISFETs are connected to drains of the second and fourth MISFETs, a source-drain path of the fifth MISFET is connected between said first bit line and the drain of the third MISFET, a source-drain path of the sixth MISFET is connected between said second bit line and the drain of the fourth MISFET,

wherein regions forming channels of the first to fourth MISFETs are in a floating state, and

wherein regions forming channels of the fifth and sixth MISFETs are coupled to a first wiring line supplying a potential.

2. (Original) The semiconductor device according to claim 1, wherein said semiconductor device is a semiconductor chip, having first and second semiconductor layers, and an insulating film provided between the first and second semiconductor layers,

wherein diffusion layers of the first to sixth MISFETs are formed in the first semiconductor layer, and

wherein regions forming channels of the first to sixth MISFETs are each separated by an insulating layer.

3. (Original) The semiconductor device according to claim 2, wherein a potential of

the region forming the channel of the fifth MISFET is controlled by a potential of a word line connected to the gate of the fifth MISFET,

a potential of the region forming the channel of the sixth MISFET is controlled by a potential of a word line connected to the gate of the sixth MISFET, and

a potential of the region forming the channels of the fifth and sixth MISFETs in a memory cell connected to a non-selected word line of the plurality of word lines is lower than the potential of the region forming the channels of the fifth and sixth MISFETs in a memory cell connected to a selected word line of the plurality of word lines.

4. (Original) The semiconductor device according to claim 2, wherein while a word line is selected and a word line is not selected, a same potential is supplied to the first wiring line.

5. (Original) The semiconductor device, according to claim 1, wherein said semiconductor device is a semiconductor chip having first and second semiconductor layers and an insulating layer in between the first and second semiconductor layers,

wherein a voltage larger than an operating voltage applied to the memory cell is applied to the second semiconductor layer,

wherein diffusion layers of the third to sixth MISFETs are formed in the first semiconductor layer, and

wherein the first and second MISFETs are vertical MISFETs, each of which has a source region, a channel region, and a drain region deposited above the first semiconductor layer.

6. (Original) A semiconductor device, comprising:

a memory cell having first and second load P-channel type MISFETs, first and second driver N-channel type MISFETs, and first and second transfer N-channel type MISFETs,

wherein gate and channel regions of the first transfer N-channel type MISFET is coupled to each another,

wherein gate and channel regions of the second transfer N-channel type MISFET are coupled to each another,

wherein gate and channel regions of the first load P-channel type MISFET are not coupled to each another,

wherein gate and channel regions of the second load P-channel type MISFET are not coupled to each another,

wherein gate and channel regions of the first driver N-channel type MISFET are not coupled to each another, and

wherein gate and channel regions of the second driver N-channel type MISFET is not coupled to each another.

7. (Original) The semiconductor device according to claim 6, further comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of said memory cells,

wherein a potential of the channel region of the first transfer N-channel type MISFET in a memory cell connected to the non-selected word line of the plurality of word lines is lower than a potential of the channel region of the first transfer N-channel type MISFET in the memory cell connected to a selected word line of the plurality of word lines, and

wherein said plurality of memory cells are formed on a SOI substrate.

8. (Original) The semiconductor device according to claim 7,

wherein a voltage larger than an operating voltage of the memory cells is applied to the SOI substrate, and

wherein the channel regions of the first and second driver N-channel type MISFETs and the first and second transfer N-channel type MISFETs are separated by insulating layers.

9 - 41 (Canceled)